HIGH-SPEED, LOW-POWER, EXCELLENT EMC: LVDS FOR ON-BOARD DATA HANDLING

Dr SM Parkes

Applied Computing, University of Dundee, Dundee, DD1 4HN, Scotland, UK

Tel: 44 1382 345194, Fax: 44 1382 345509, Email: sparkes@computing.dundee.ac.uk

ABSTRACT

The capabilities of remote-sensing instrumentation are developing rapidly. As a consequence the data rates being handled on-board spacecraft are increasing.

LVDS (Low Voltage Differential Signaling) provides a means of sending data along a twisted pair cable at high speed, with low power and with excellent EMC performance. These features make LVDS ideal for satellite on-board data-handling applications.

This paper assesses the suitability of LVDS for space applications as part of a data-handling system based on IEEE 1355 comparing it against other types of line driver/receiver. It explains how LVDS can be used together with IEEE 1355 to form the basis for a powerful on-board data handling system, which is capable of handling data from current and future, high data-rate instruments.

1 INTRODUCTION

1.1 Background

The IEEE 1355 standard (Ref. 1) was selected for use in space-based signal and image processing and data handling systems at the ESA "Open Interface Data Link" round table meeting (Ref. 2). Following a detailed analysis of available inter-processor communication methods (Ref. 3) the merits of the IEEE 1355 standard were clear:-

- it was a bi-directional, high speed (>100Mbits/sec), serial interface standard;
- it could be used in single-ended mode over short distances connecting components on a PCB or boards within a box, and in a differential mode over longer distances (10m+) between boxes;
- each bi-directional link operating at > 100Mbits/sec in each direction required four wires single-ended and eight wires differential;
- the low-level interface was extremely simple requiring around 5000 gates for an interface (a similar complexity to a USART), this level of complexity meant that the interface could be readily implemented in radiation tolerant, space-qualifiable technology;
- an effective flow-control mechanism had been devised which supported low-latency communication;
- higher-level message routing protocols and supporting components were under development;
- fault tolerant systems became easy to construct.

Since the endorsement of the IEEE 1355 by ESA and major companies involved in the space industry, the technology has been migrated successfully into radiation-tolerant, space-qualifiable components. Daimler-Benz Aerospace and TEMIC have developed a component (SMCS) which provides three IEEE 1355 compatible links and a processor interface (Ref. 4). Demonstration systems have been and are being developed for both multi-DSP processing systems (Ref. 5) and for large capacity, solid-state data storage systems (Ref. 6). High level protocols have been developed to support interprocessor communication (Ref. 7). Software support for the SMCS link devices has been provided within the Eonic Virtuoso real-time operating system for both the TSC21020 DSP processor and the ERC32 SPARC 32-bit processor (Ref. 8).

The Digital Interface Circuit Evaluation (DICE) study was initiated by ESTEC to take stock of these developments, to assess the current state of "Open Interface Data Link" components, to identify what elements of the communication system are missing or inadequate and to go on to develop those elements.

1.2 Data Link Requirements Overview

An overview of the main physical and signalling requirements for a data link for use in space applications are listed below.

- **Data Rate:** A data link must have sufficient capacity or bandwidth to carry the data for which it was intended. 100Mbaud is an appropriate minimum target data rate.
- **Distance:** The data link must operate over a distance of 10m. This distance is commensurate with the size of a large spacecraft enabling data to be transmitted from one extremity to the other.
- **Power Consumption:** The power consumption of the link should be low.
- **Scalability:** To meet the data rate requirements of particularly demanding applications it must be possible to use several links in parallel without the need for new protocols.
- **Error Rate:** The error rate on the link should be low, better than a BER (bit error rate) of 10^{-12} for the basic link and better than 10^{-14} for a link protected by a higher level error detection protocol.
- **EM Susceptibility:** The data link should not be susceptible to interference from external electromagnetic sources
- **EM Emission:** The data link should not emit electromagnetic radiation at a level that would interfere with the operation of other systems.

- **Magnetic Emission:** Magnetic emissions from the data link must be low – ferrous materials should not be used in the data link components.
- **Galvanic Isolation:** It should be possible to galvanically isolate the data transmission system from the data reception system.
- **ESD Immunity:** The electronic devices forming a link shall have a high level of immunity to damage by electro-static discharge.
- **Radiation Tolerance:** The components that implement the data link should be tolerant of radiation.
- **Low mass and small size:** The mass and size of the data link interface and the cable should be as small as possible.
- **Cold Redundancy:** The data link should support connection within a cold redundant system, i.e. when part of the system is powered and another part is not powered.

Detailed requirements are listed in table 3 at the end of this paper.

2 IEEE 1355 STANDARD

In this section an overview of the IEEE-1355 standard is presented and the problems with using it in a space application are examined.

2.1 Overview

IEEE 1355-1995 includes several different point-to-point communication standards:

- DS-SE (Data-Strobe, Single-Ended) uses Data-Strobe (DS) encoding and single-ended CMOS or TTL level signals. It is intended for use on PCBs or between boards over short distances (<1m) at a data rate of up to 200 Mbaud.
- DS-DE (Data-Strobe, Differential Ended) uses Data-Strobe encoding and differential pseudo-ECL (PECL) signals. It is intended for use between PCBs and between units over distances of up to 10m at a data rate of up to 200 Mbaud. DS-DE is the same as DS-SE except for the use of the differential PECL signals rather that CMOS or TTL level signals.
- TS-FO-02 (Three-of-Six, Fibre-Optic) uses two fibre optic cores in a cable to provide bi-directional communication with one fibre transmitting in one direction and the other in the opposite direction. It employs a three-of-six code where each valid six-bit symbol has three ones and three zeros. TS-FO-02 operates at a maximum of 250 Mbaud over a maximum distance of 300m.
- HS-SE-10 (High-Speed, Single-Ended) uses two 50 ohm coaxial cores in one cable to provide bi-directional communication with one coaxial core transmitting in one direction and the other in the opposite direction. It employs an 8B/12B code which is DC balanced. HS-SE-10 has an operating speed between 700 Mbaud and 1Gbaud and operates over distances of up to 8m.
- HS-FO-10 (High-Speed, Fibre-Optic) uses two fibre optic cores in a cable, one for transmission in each direction. The encoding used is identical to the HS-SE-10 specification. HS-FO-10 will operate over maximum distances of 100 – 3000m depending upon the type of optical fibre used.

The part of the IEEE1355-1995 standard being considered for space applications is DS-DE. Since DS-DE is a differential-ended version of DS-SE, the DS-SE specification will be considered first followed by DS-DE.

2.1.1 DS-SE

DS-SE and DS-DE links are point to point communication links which operate over transmission lines on a PCB or within a cable. DS-SE and DS-DE use a coding scheme which encodes the transmission clock with the data into data and strobe so that the clock can be recovered by simply XORing the data and strobe lines together. The data values are transmitted directly and the strobe signal changes state whenever the data remains constant from one data bit interval to the next. This coding scheme is illustrated below in figure 1. The DS encoding scheme is also used in the IEEE 1394-1995 (Firewire) standard (Ref. 9).

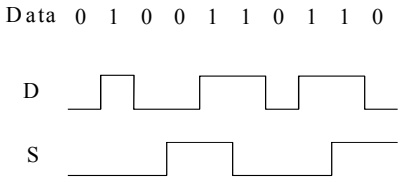

Figure 1 : Data-Strobe (DS) Encoding

A DS-SE link comprises two pairs of wires, one pair transmitting the D and S signals in one direction and the other pair transmitting D and S in the opposite direction. That is a total of four wires for each bi-directional link.

DS-SE is designed to use standard TTL output and input levels operating over a 50 ohm or 100 ohm transmission line. The driver output impedance is used to terminate reflections from the receiver so must be matched to the impedance of the transmission line when the output is high or low, and when the output is switching.

The receiver input impedance is high so that the transmitted signal is reflected by the receiver – this is to ensure a clean transition at the receiver input. The reflected signal must be terminated at the transmitter.

2.1.2 DS-DE

DS-SE is designed for communication between devices on a PCB or between boards. DS-DE is an adaptation of DS-SE that is capable of transmitting data reliably between boxes over distances of up to 10m.

The single-ended, TTL compatible signals of DS-SE are replaced by differential, pseudo-ECL (PECL) compatible signals. Differential (PECL) provides the required high signalling rate reliably over long distances (up to 10m). The number of wires needed is now eight for each bi-directional

link. The use of PECL significantly increases link power consumption.

2.1.3 DS-SE and DS-DE Character Level

DS-SE and DS-DE share the higher level protocols including character level and exchange levels which are defined in IEEE 1355-1995.

There are two types of characters:-

- Data characters which hold an eight-bit data value, transmitted least-significant bit first. Each data character contains a parity-bit, a data-control flag and the eight-bits of data. The parity-bit covers the previous eight-bits of data, the current parity-bit and the current data-control flag. It is set to produce odd parity so that the total number of 1's in the field covered is an odd number. The data-control flag is set to zero to indicate that the current character is a data character.
- Control characters which hold a two-bit control code. Each control character is formed from a parity-bit, a data-control flag and the two-bit control code. The data-control flag is set to one to indicate that the current character is a control character. Parity coverage is similar to that for a data character. One of the four possible control characters is the escape code (ESC). This can be used to form longer control codes. One longer control code is specified in IEEE 1355-1995 which is the NULL code. NULL is formed from ESC followed by the flow control character (FCC). NULL is transmitted whenever a link is not sending data or control tokens to keep the link active and to support link disconnect detection.

The data characters, control characters and parity coverage are illustrated in figures 2 and 3.

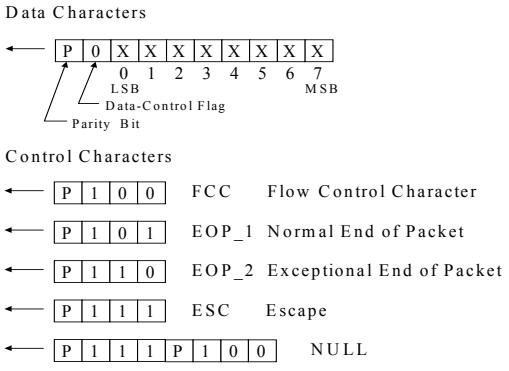

Figure 2 : Data and Control Characters

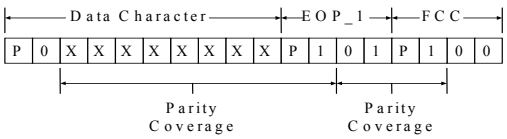

Figure 3 : Parity Coverage

2.1.4 DS-SE and DS-DE Exchange Level

An exchange level protocol is defined in IEEE 1355-1995 which provides the following services:-

- **Initialisation:** Following reset the link output is held in the reset state until it is instructed to begin transmission. The link output then starts to transmit NULL characters and the link input is monitored for the reception of a character. Once a valid character has been received on the input then the output can start normal operation.
- **Flow Control:** A transmitter is only allowed to transmit data characters if there is space in the receiver buffer for them. The receiver indicates that there is space for eight more data characters by sending a flow control character (FCC). If multiple FCC's are received then it means that there is a corresponding amount of space available in the receiver buffer e.g. four FCC's means that there is room for 32 data characters.
- **Detection of Disconnect Errors:** Link disconnection is detected when following reception of a data bit no new data bit is received within a link disconnect timeout window. IEEE 1355-1995 defines the link disconnect timeout window to be 850ns. Once a disconnection error has been detected the link attempts to restart (see below).
- **Detection of Parity Errors:** Parity errors occuring within a data or control character are detected when the next character is sent, since the parity bit for a data or control token is contained in the next character. Once a parity error has been detected the link will attempt to restart (see below).
- **Link Restart:** Following an error or reset the link attempts to re-synchronise and restart using an "exchange of silence" protocol. The end of the link that is reset or where the error is detected ceases transmission. This is detected at the other end of the link as a link disconnect and that end stops transmitting too. The first link resets its input and output for 6.4 usec and the other end will do likewise. Each link then waits a further 12.8 usec before starting to transmit. These periods of time are sufficient to ensure that the two links are resynchronised and ready to receive data.

2.2 IEEE 1355 Components

A brief description of the each of the known IEEE-1355 compatible devices will now be given.

2.2.1 STM C101

The C101 is the IEEE 1355 DS link interface produced by SGS Thomson (formerly Inmos). STM have ceased manufacturing this device.

2.2.2 STM C104

The STC104 is a packet routing switch for IEEE 1355 DS packets. STM have ceased manufacturing this device.

2.2.3 STM Macro-Cell

STM have made available (under licence) the DS link interface as an ASIC macrocell for use in ASIC

implementations. None of the IEEE-1355 devices produced by other manufacturers use the STM macrocell to the knowledge of the author.

2.2.4 DSS SMCS332

The DSS (Dornier Satellitensysteme) SMCS332 (Scalable Multi-Channel Communication Subsystem) implements three DS links operating at 200Mbps together with a 8, 16 or 32-bit processor interface in a radiation tolerant ASIC device. It features standardised high-level protocol extensions to support its application in fault tolerant systems, heterogeneous architectures as well as implementing power saving features. These include control by link, dual endian support, and checksum generation / detection features. Power consumption ranges from 600mW with all three links at 140Mbps to 200mW with links at 10Mbps. The SMCS332 is available now (Rev. B). MHS intends to release this version under licence from DSS.

2.2.5 DSS SMCSLite

The DSS SMCSlite is being implemented to provide the means of interfacing a non-intelligent front-end or other device to a single DS link. The device is expected to operate at up to 200Mbps and is being implemented as a compact radiation tolerant 100 pin ASIC in MHS technology. The SMCSlite includes circuitry for command execution and protocol generation, thereby simplifying the interface with non-intelligent subsystems. Additional on-chip facilities include timers, FIFO control, ADC/DAC interfaces, UARTS, etc. The power consumption of the SMCSlite is estimated to be 200mW at 140Mbps and 70mW at 10Mbps. Availability is scheduled for 98Q3.

2.2.6 DSS CIA FPGA

The DSS CIA (Communication Interface Adapter) was designed for use in a Solid State Mass Memory (SSMM) system. It provides a single 50Mbps IEEE 1355 DS link interface in an Actel A1280 FPGA device. The CIA contains 16-byte input and 2-byte output buffers. An 8/16-bit is provided for CPU control and communication. In parallel there is a 9 bit input and a 9 bit output FIFO data port for high speed communication (50 MBit/s). The data rate is limited by the technology used. Its power consumption is about 900 mW at 50 MBit/s due to clock path restrictions of the FPGA technology.

2.2.7 DSS CSM FPGA

The DSS CSM (Communication Switching Matrix) is a crossbar switching element. It provides 16 inputs and outputs and may be used as an element to build larger crossbar switches. The device is a static crossbar switch. The CSM is implemented by means of two Actel 1280 FPGA devices and is now being transferred to a gate array implementation.

2.2.8 4-Links C111

The 4-Links C111 is a PLD implementation of a single DS-Link which requires external transmit and receive FIFOs.

2.2.9 MMS FPGA

The MMS DS-Link FPGA is a Xilinx 3095-3 implementation of a single IEEE 1355 DS-link which operates at the full 100Mbps (Ref. 3). It contains 16-byte input FIFO and a 12-byte output FIFO and uses a 9-bit parallel input/output port to provide 8-bit data and commands. The device is housed in a 160 pin quad flat pack, operates at 5 volts and uses a 50MHz clock. This design is not available outside Matra Marconi Space.

2.2.10 NTU Devices

The Parallel Processing and Research Group of Nottingham Trent University (NTU) have designed and fabricated a 16 link dynamic routing device the ICR C416. This interfaces to INMOS OS Links of T2,4,8 processors. The group has also designed, using VHDL tools, a new routing device which supports both uni and multi-cast messages.

2.3 Problems

There are several problems with using IEEE-1355 for space applications.

1. The DS-DE signalling for IEEE-1355 uses differential PECL drivers and receivers. The problem with PECL is its relatively high power consumption (around 500mW for a bi-directional IEEE-1355 link). The AT&T AT41 drivers/receivers recommended in IEEE-1355 are only commercial grade and their continued availability is uncertain. An alternative high-speed differential signalling method is required which operates at lower power than PECL and which is suitable for space-qualification.
2. The connectors as defined in the IEEE1355-1995 standard are not suitable for space application. They were designed for use on a PC interface card. They are long and thin to penetrate the PC card front panel and to allow stacking of several connectors next to each other in the limited space available on a PC card front panel. These attractive features for a PC card connector make it mechanically unstable and unsuitable for a space applications. The use of an existing space-qualified connector, if possible, would avoid the cost of development and qualification.
3. The cables as defined in the IEEE1355 standard may be suitable, but a better quality cable (lower resistance wire, category 5) would give improved performance especially over long (10m) cable lengths.
4. The availability of effective message routing switches is fundamental to IEEE-1355 applications. The STM C104 switch is no longer being manufactured. An alternative that can be implemented in a radiation tolerant process is needed.
5. IEEE 1355-1995 is actually several different communication standards in one – none of which are suitable for space application as they stand. A new standard based on the DS-DE part of IEEE 1355-1995 is needed specifically for space applications. This may be a revision to IEEE 1355-1995 or a separate ESA standard.

The first three problems need to be addressed before the IEEE-1355 can be used as a standard for space applications.

The fourth problem will become important only after the components needed to build the basic point-to-point data link have been developed. The fifth problem is readily overcome once the other have been addressed.

3 DIFFERENTIAL DRIVER/RECEIVER TECHNOLOGY

This section addresses the driver and receiver technology that is required for the data link. First the concept of differential signalling is introduced and then ECL and LVDS driver/receiver technologies are considered. Finally ECL and LVDS are compared.

3.1 Differential Signalling

Differential signalling overcomes many EMC problems by eliminating signal return current. Two signals are transmitted: the wanted signal and its negative. The return currents from these two signals cancel one another out. If the differential signals are not exactly opposite (well balanced) then a small return current (the common mode current) will be produced. Low return currents and hence low common mode currents are important for good EMC performance.

To ensure that the return currents from the two signals cancel it is important that the two signals follow the same path (see figure 4). Hence PCB traces should be routed close together, adjacent connector pins should be used for differential pairs and twisted pair cable should be used.

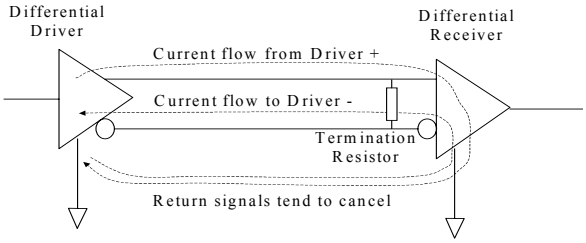

Figure 4 : Return Signal in Differential Signalling

The required signal is reconstructed by comparing the two complementary signals. Any ground voltage shift between the driver and receiver is common to both of the differential signal lines and affects them both equally. Thus ground voltage shifts have no effect on differential signal reception (provided that the input voltage range of the receiver is not exceeded). Ref. 10.

ECL (Emitter Coupled Logic) and LVDS are two technologies which can provide high-speed differential signalling. Each will be considered in turn.

3.2 ECL/PECL/LVPECL

3.2.1 ECL

ECL (Emitter Coupled Logic) is a high speed logic family which has low output impedance, high current drive capability and high input impedance. These characteristics make ECL devices ideal for transmission line driving. Complementary outputs with equal propagation delay, provided on many ECL components, means that they are able to produce differential signals for driving twisted pair transmission lines over long distances. ECL line receivers have a differential threshold of a few hundred millivolts and common mode rejection of 1 volt or more.

A differential amplifier design is used in ECL outputs which steers the output current between two paths rather than switching it on and off. ECL devices thus have a power supply current drain which is independent of the logic state and frequency of operation. This results in much reduced switching noise on the power supply rails when compared to voltage switching devices like CMOS or TTL.

ECL logic is designed to operate with negative power supplies (i.e. VCC connected to ground). All the ECL internal switching references and output levels are derived from VCC. Any noise on the VCC line will thus couple directly into the switching references and output levels, so it is important that VCC has as low noise as possible. This is the reason that ECL usually runs off a negative (-5.2 volt) supply with VCC connected to ground. ECL will, however, work with positive power supplies provided that the supplies are stable and low noise.

3.2.2 PECL

Positive ECL (PECL) refers to standard ECL components run off a positive (+5 volt) supply. The advantage of running ECL off a +5 volt supply is that it can work off the same supply as other logic devices in a system removing the need for an additional -5.2 volt supply.

Recent ECL families are voltage compensated which means that they can operate with a wider supply voltage enabling +5 volt operation (Ref. 11). ECL families which are not voltage compensated (e.g. 10K family) cannot be used as PECL.

In a PECL design, the need to keep noise on the VCC supply to a minimum is reduced in a differential design because the VCC noise is common mode and is rejected by the differential receiver input. It is still important that the VCC rail is kept as stable and noise free as possible and separate VCC sub-planes should be used for CMOS/TTL logic and PECL.

Differential PECL (or ECL) can be terminated simply with a single resistor across the two receiver inputs. PECL/ECL is able to cope with a range of line impedances from 50 ohm to 130 ohm. The value of the termination resistor should match the line impedance.

If PECL is used in a system where the receiver can be powered down while the driver is powered, a serious problem can result. The base-collector junction of the receiver input transistor will be forward biased and can conduct enough current through the collector load resistor to damage the device.

3.2.3 LVPECL

One of the main uses for PECL devices is in clock distribution circuits for CMOS/TTL based systems. PECL devices are low skew, high speed components which are ideal for clock distribution. Low voltage PECL was introduced to be compatible with low voltage CMOS/TTL circuitry so that PECL could be used in 3.3V systems. The low voltage operation gave a small power consumption gain in the static

device power consumption but no advantage in the power consumption of the output transistors. This is because the device thresholds relative to the operating supply Vcc remain the same.

3.3 LVDS

3.3.1 Overview

LVDS stands for Low Voltage Differential Signalling (Ref. 12, 13). It uses balanced signals to provide very high-speed interconnection using a low voltage swing (400mV maximum). The balanced or differential signalling provides adequate noise margin to enable low voltages to be used in practical systems. Low voltage swing means low power consumption at high speed.

LVDS is appropriate for connections between boards in a unit, and unit to unit interconnections over distances of 10m or more. Various forms of interconnection can be used: PCB tracks, backplane, and cables.

LVDS has several features that make it very attractive for data signalling:-

- Power consumption is typically 50mW per driver/receiver pair for LVDS compared to 120mW for ECL.
- A properly terminated twisted pair cable can be driven with LVDS over 10m at speeds greater than 100Mbps, depending on allowable jitter in the receiver/decoder.
- Simple 100 ohm termination at receiver.
- Near constant total drive current (+3.5mA for logic 1 and -3.5mA for logic 0) which decreases switching noise on power supplies.
- High immunity to ground potential difference between driver and receiver - LVDS can tolerate at least ±1V ground difference.
- High immunity to induced noise because of differential signaling normally using twisted-pair cable.
- Low EMI because small equal and opposite currents create small electromagnetic fields which tend to cancel one another out.
- Not dependent upon particular device supply voltage(s).
- Failsafe operation - the receiver output goes to the high state (inactive) whenever
    - the receiver is powered and the driver is not powered,
    - the inputs short together,
    - input wires are disconnected.
- Failsafe operation - if an LVDS driver is powered but the receiver is not powered (a situation that could possibly arise in cold redundant systems) then the ESD protection diode at the receiver input will provide a low impedance path to ground and the signal line will be clamped to one diode drop above ground. Current will then flow through the ESD protection diode. With LVDS drivers the short circuit current limit is low enough to prevent subsequent thermal damage in the receiver.

A typical LVDS driver and receiver are shown in figure 5, connected by a media (cable or PCB trace) with 100 ohm differential impedance.

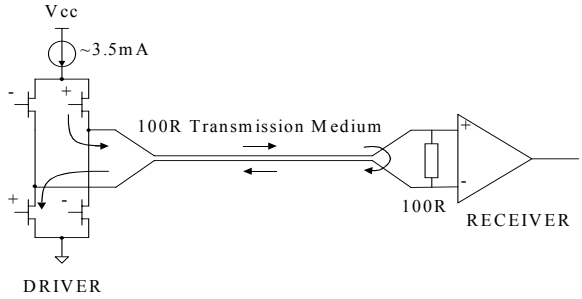

Figure 5 : LVDS Driver and Receiver

The LVDS driver uses current mode logic. A constant current source of around 3.5mA provides the current that flows out of the driver, along the transmission medium, through the 100-ohm termination resistance and back to the driver via the transmission medium. Two pairs of transistor switches in the driver control the direction of the current flow through the termination resistor. When the driver transistors marked "+" in figure 4-2 are turned on and those marked "-" are turned off, current flows as indicated by the arrows on the diagram creating a positive voltage across the termination resistor. When the two driver transistors, marked "-", are turned on and those marked "+" are turned off, current flows in the opposite direction producing a negative voltage across the termination resistor. LVDS receivers are specified to have high input impedance so that most of the current will flow through the termination resistor to generate around ±350mV with the nominal 3.5mA current source.

The current mode switching means that the driver power supply current is almost constant: the current source is either supplying the "+" pair of output transistors or the "-" pair. This results in a power supply current that does not change dramatically with increasing operating frequency, as is the case with voltage switching methods (CMOS and TTL).

The low voltage levels used means that data can be switched quickly giving high speed and that the power consumption is low at high operating frequencies.

3.3.2 LVDS Standards

There are two standards which define LVDS:-

1. TIA/EIA-644 that defines the driver output characteristics and the receiver input characteristics only.
2. IEEE 1596.3 Low Voltage Differential Signaling (LVDS) for Scalable Coherent Interface (SCI) that defines the signalling levels used and the encoding for packet switching used in SCI data transfers.

3.3.2.1 ANSI/TIA/EIA-644-1995 (Ref. 12)

TIA stands for Telecommunications Industry Association and EIA for Electronic Industries Association. ANSI is the American National Standard Institute. The ANSI/TIA/EIA-644-1995 standard is referred to as the EIA-644 standard throughout this paper.

The EIA-644 standard specifies low voltage differential signalling drivers and receivers suitable for high speed data communications purposes. High-speed, low-power, low-EMI and implementation flexibility were the main factors in driving the specification.

The drivers and receivers specified are capable of operating at data signalling rates of up to 655Mbits/s. The low voltage signalling level adopted results in low power consumption. Differential operation gives rise to low EMI. The signalling technique was specified to allow operation independent of power supply voltage and so may be implemented in a variety of integrated circuit technologies. Standard IC power supplies of 5V or 3.3V can be used and a power supply as low as 2.5V can be accomodated.

3.3.2.2 IEEE 1596.3-1996 (Ref. 13)

The IEEE 1596.3 standard forms part of the IEEE 1596 Scalable Coherent Interface (SCI) standard. SCI is a high-speed packet transmission protocol aimed at parallel processing systems. The initial definition of SCI specified ECL drivers for the high speed interface. This led to problems with power consumption in the data communication interfaces. IEEE 1596.3 was developed to overcome the problems with ECL power consumption in SCI applications. To reduce power consumption while retaining high speed operation, a lower voltage swing is required than provided by ECL.

IEEE 1596.3 provides two similar low voltage differential signalling driver and receiver specifications. One for use across backplanes where the potential difference between grounds at the driver and receiver is less than 50mV. The other is for systems connected via cable where the potential difference between grounds can be significant. In this case a ground difference of ±1 V can be tolerated.

IEEE 1596.3 also provides a specification for data encoding to support the transfer of SCI packets across various data path widths. Only the driver and receiver specifications of IEEE 1596.3 are of interest here.

3.3.2.3 Differences Between EIA-644 and IEEE-1596.3

Close inspection of the EIA-644 and IEEE-1596.3 standards reveals several differences:-

- trise and tfall : IEEE 1596.3 is aimed at higher speed (500Mbaud) applications only whereas EIA-644 is aimed at lower speeds as well. EIA-644 has a more relaxed trise and tfall specification for lower speed operation.
- Output differential voltage : The maximum specification is slightly lower for IEEE-1596.3. This, it seems, is so that 2V power supplies can be used.
- Output offset voltage : The maximum output offset voltage for IEEE-1596.3 is lower than that for EIA-644. Again, this is so that 2V power supplies can be used.
- Delta Vod, Delta Vos : EIA-644 has a more relaxed requirement for the balance of Vod and Vos as the driver switches between “1” and “0”.
- Receiver differential input impedance : IEEE-1596.3 has a more stringent requirement probably because of its higher operating speed.

These differences are minor and manufacturers of LVDS devices claim compatibility with both EIA-644 and IEEE-1596.3. The same devices may also be used for IEEE-1394.

3.3.2.4 IEEE 1394-1995 (Ref. 9)

The IEEE 1394-1995 standard for a high performance serial bus also uses low-voltage differential signalling, but at a different level to EIA-644 and IEEE-1596.3.

The IEEE 1394-1995 standard, also known as firewire, was developed as a high-speed peripheral bus. It is being widely adopted as a means of connecting peripherals to a PC, including digital video recorders, digital cameras, camcorders, printers and scanners. This standard is of interest because it uses low voltage differential signalling techniques. The differential signalling levels employed are similar to the backplane specification of the IEEE 1596.3 standard, but they are intended to be used over cables of up to 4.5m in length.

IEEE 1394 defines a complete serial bus standard, from cables and connectors, through physical signalling levels and low-level signalling protocols, up to service layer protocols. It is worth noting that the IEEE 1394 uses the same Data-Strobe encoding technique as IEEE 1355.

3.4 Comparison of PECL and LVDS

In this section PECL and LVDS are compared.

The following table (table 1) provides a comparison of PECL and LVDS, both operating at 5V and 3.3V. For comparison purposes a 100 ohm simple termination is assumed for both PECL and LVDS.

Table 1 : PECL and LVPECL versus LVDS

Technology	PECL (10E)	LVPECL (100LVE)	LVDS	LVDS
Supply Voltage	5 V	3.3 V	5 V	3.3 V
Differential Driver Output Voltage	±750 mV	±750 mV	±450 mV	±450 mV
Receiver Input Threshold	± 310mV	±270 mV	±100 mV	±100 mV
Data Rate (MBps)	> 400	> 400	> 400	> 400
Quad Driver Device Power, No Load	200 mW	132 mW	33mW	66 mW
Quad Receiver Device Power	200 mW	132 mW	55 mW	59 mW
Single 100 ohm Load Current	7.5mW	7.5mW	4.5mW	4.5mW
Power, Single Driver / Receiver Pair	138 mW	91 mW	44 mW	46 mW
Common Mode Range	±1.7 V	±1.0 V	±1.0	±1.0 V

The main difference is in the power consumption with LVDS requiring half of the power of LVPECL and one third that of PECL.

The lower switching levels of LVDS provide better EM emission characteristics whereas the higher receiver thresholds of ECL provide better EM immunity.

The common mode voltage range for PECL is better than LVDS allowing operation between systems with a larger potential difference between grounds.

LVDS has the capability of operating with a 2.5V power supply, which is not possible with ECL.

LVDS can be implemented in different technologies (CMOS, BiCMOS, GaAs) whereas ECL is a bipolar technology. The technology independence and low power consumption of LVDS means that drivers and receivers can be integrated with other system functions e.g. IEEE-1355 encoder and decoder. LVDS could be implemented in a radiation hard CMOS or GaAs technology.

If an LVDS driver is powered but the receiver is not powered (a situation that could possibly arise in cold redundant systems) then the ESD protection diode at the receiver input will provide a low impedance path to ground and the signal line will be clamped to one diode drop above ground. Current will then flow through the ESD protection diode. With LVDS drivers the short circuit current limit is around 4mA (24mA maximum) which is low enough to prevent subsequent thermal damage in the receiver. A PECL receiver that is not powered would be damaged if driven by an active PECL driver.

In summary LVDS offers the speed of ECL at a third of the power consumption. With properly designed cables and connectors LVDS should provide adequate EMC for space applications (this is being tested in the DICE study). LVDS has significant implementation advantages.

4 SIGNAL QUALITY : DATA RATE AND LENGTH OF CABLE

This section considers the question of how far can a high-speed signal be transmitted along a cable and still be received free from error.

The length of cable that can be used to transmit data reliably at a particular data rate will depend upon signal quality and the data encoding method used.

Signal quality depends on many factors: cables, connectors, PCB traces, driver and receiver circuits

Signal quality is determined by the amplitude and timing degradation caused as it propagates from encoder to decoder.

Amplitude degradation is caused by resistive losses in the cable. For successful signal reception the differential signal level at the receiver level must be greater than the minimum receiver threshold plus the differential noise at the receiver. The cable impedance characteristics will cause greater signal attenuation at higher frequencies.

Timing degradation has two components: jitter and skew. Jitter is the time uncertainty of a high-low or low-high edge measured with respect to other edges in that signal. It is caused by inter-symbol interference, noise added to the signal and the slowing of edges through the cable etc. Skew is the timing difference caused between two signals as they propagate from source to destination. Any difference in path length will cause skew between the two signals.

Jitter is normally measured using eye pattern measurements while random data is being transmitted. It is important that the worst-case maximum jitter is measured at the LVDS receiver thresholds (±100mV). This is illustrated in figure 6.

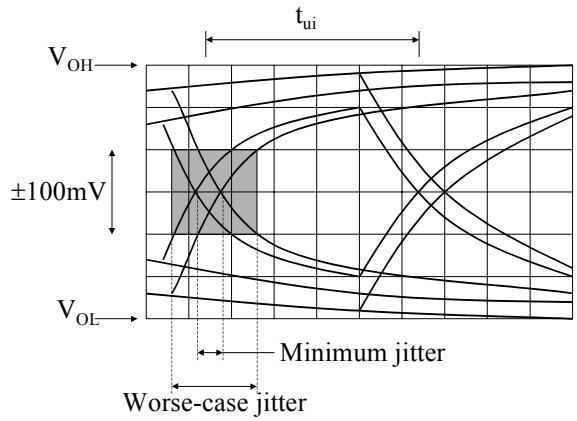

Figure 6 : Worse-Case Jitter Measured with Eye Pattern

The allowable jitter will depend upon the encoding method used and the implementation of the encoder and decoder. Consider a typical IEEE 1355 DS encoded signal as shown in figure 7.

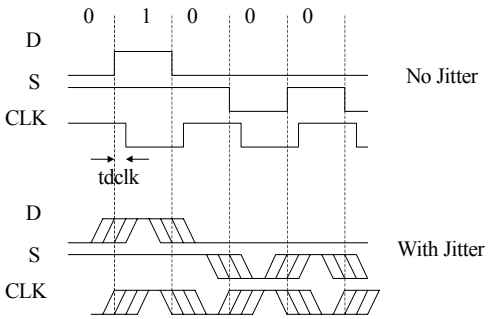

Figure 7 : Jitter on an IEEE 1355 DS Encoded Signal

The strobe signal (S) changes state at the end of the unit interval whenever the data line (D) does not. The clock signal (CLK) is derived by XORing the data (D) and strobe (S) lines together and is used to clock the value of the data line (D) into the receiver input register. There is a delay (tdclk) from the active edge of D or S to the edge of the clock signal. Both edges of the clock signal are used to clock data into the receiver register.

Jitter on the D and S signals are translated directly to the CLK line used to register the data in the decoder. If the jitter is too large then the data may be registered after it has started to change as shown in figure 8 below.

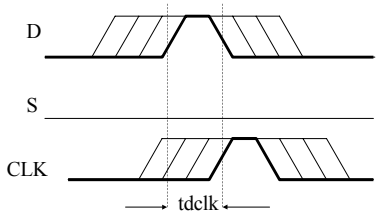

Figure 8 : Jitter Causes Invalid Data to be Registered

The thick lines in figure 8 show the assumed worst case jitter. The clock edge produced from the rising edge of D is delayed by a time tdclk. This is the delay through the clock extraction logic in the decoder. By the time the clock signal goes high the data has started to change so invalid data may be received. Any required data hold time must also be allowed for.

The delay from D or S to the clock signal is dependent upon the implementation of the receiver. The worst case delay to the clock signal is given by

$$t_{dclk} = \text{Max}\{t_{DCLKL}, t_{DCLKH}, t_{SCLKL}, t_{SCLKH}\}$$

where t_{DCLKL} is the delay from an edge of D to the clock going low, etc.

The requirements on the maximum jitter are then given by

$$\text{Jitter on D or S, } t_{JITTER} < t_{ui} - t_{dclk} - t_{hold}$$

Where t_{ui} is the unit interval, or data signalling period.

It is also necessary to consider the skew between D and S, t_{DSSKEW}. Then the jitter requirements become

$$\text{Jitter on D or S, } t_{JITTER} < t_{ui} - t_{dclk} - t_{hold} - t_{DSSKEW}$$

This timing requirement is illustrated in figure 9 below.

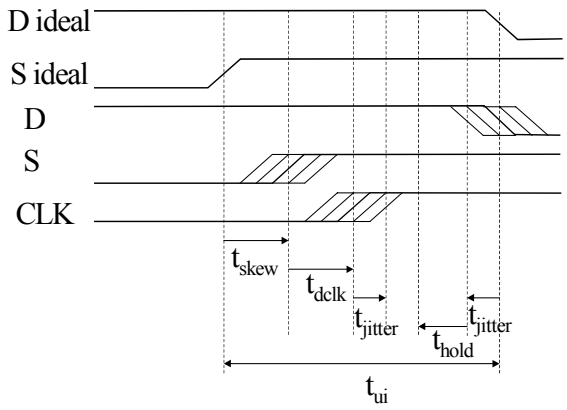

Figure 9 : Timing Requirements for DS Decoder

The timing margin is given by

$$\text{Margin} = t_{ui} - t_{dclk} - t_{hold} - t_{DSSKEW} - t_{JITTER}$$

The IEEE-1355 specification provides a timing specification for the encoder D-S skew (maximum) and for the decoder D-S skew requirement (maximum). Using the skew values quoted in the National Instruments DS90C031/032 LVDS driver and receiver data sheets (Ref. 14, 15) and an estimate of the connector/cable jitter/skew, the timing margin for operation at 100Mbaud can be estimated. This estimate is provided in table 2 below.

Table 2: Estimation of Jitter/Skew Margin for IEEE-1355 System

Signal Path	Source of information	**Time (ns)**
1355 Encoder output skew, t_{DSO}	IEEE-1355 specification	2.5
Driver max. channel-channel skew, t_{SK1}	Nat. Semi. DS90C031 Data Sheet	1.0
Cable and connector jitter (maximum jitter at ±100mV levels)	Nat. Semi. LVDS Owner's Manual	2.0 (at 10m)
Receiver max. channel-channel skew, t_{SK1}	Nat. Semi. DS90C032 Data Sheet	1.5
1355 Decoder max. input skew, t_{DSI}	IEEE-1355 specification	2 (i.e. ±1)
Total		9
Margin at 100Mbaud		1

5 LVDS DEVICES

A range of LVDS driver and receiver devices are available from National Semiconductor (Ref. 14, 15) and Texas Instruments (Ref. 18, 19). National Semiconductor do a wide range of LVDS devices operating at different speeds, at different supply voltages, with various numbers of drivers and receivers in a package. LSI Logic provide the Hyper-LVDS I/O cell for their LCB500K CMOS ASICs (Ref. 20).

None of these devices are currently space qualified. If necessary, LVDS drivers and receivers could be manufactured in a radiation tolerant CMOS technology.

6 DOES LVDS MEET THE REQUIREMENTS

This section attempts an initial evaluation of LVDS against data link requirements that were summarised in the introduction to this paper. The requirements are detailed in table 3 at the end of this paper. The EMC requirements are intended to be in line with those of ENVISAT and Rosetta (Ref. 16, 17).

Table 3 lists the requirements and considers whether LVDS is likely to meet each requirement for the data link. A tick (√) in the table means that it is thought that LVDS is likely to meet a requirement. TBC in the table means that LVDS will be tested against the requirement during the current DICE study.

In summary LVDS looks very promising for space applications. It is expected to meet all the requirements for the high-speed, low-power data link for space applications.

7 CONCLUSIONS

The physical and signalling requirements for a high-speed serial data link for use on-board a spacecraft were summarised in the introduction.

The IEEE 1355-1995 standard has been reviewed and its shortcoming for space applications identified. The DS-DE part of IEEE 1355 is the most relevant but its use of differential PECL drivers and receivers leads to an unacceptably high power consumption. The connectors specified in IEEE 1355 are not suitable for space use.

The use of differential signalling to provide high-speed data communication with low EMI was explored. ECL, PECL and LVPECL technologies were examined together with LVDS. In comparing LVDS with the ECL technologies LVDS was a clear winner on power consumption, implementation in different technologies, EM emission and use in cold redundant system. PECL has an advantage in better immunity to EMI.

The factors affecting the performance (speed versus distance) of LVDS were considered and the importance of controlling skew and jitter stressed. Calculations showed that DS90C031/2 driver and receiver devices should be able to support IEEE 1355 DS-DE type data communication at a maximum rate of at least 100Mbaud over a distance of 10m.

The expected performance of LVDS / IEEE 1355 DS-DE was reviewed against the requirements for the high-speed data link. Areas where testing or characterisation will be performed during the remainder of the DICE study were identified. In summary it is anticipated that LVDS / IEEE 1355 DS-DE will meet all the requirements. Radiation tolerance of existing devices is one area of concern – but if current LVDS devices are not sufficiently radiation tolerant then the LVDS drivers and receivers could be manufactured in radiation tolerant technology. One of the attractions of LVDS is that it can be implemented in a wide range of different technologies.

8 ACKNOWLEDGEMENTS

The Author would like to acknowledge the support of ESA for the Digital Interface Circuit Evaluation study, ESA Contract No. 12693/97/NL/FM, on which this paper is based The assistance of J. Rosello, the ESA study technical manager has been appreciated. Advice from Dornier Satellitensysteme, in particular T. Pike, and Patria Finavitec has also been appreciated.

9 REFERENCES

1. IEEE Computer Society, "IEEE Standard for Heterogeneous Interconnect (HIC) (Low-Cost, Low-Latency Scalable Serial Interconnect for Parallel System Construction)", IEEE Standard 1355-1995, IEEE, June 1996.

2. ESA 1995, Proceedings 'Open Interface Data Link' Round Table, WSP/PP/68, ESTEC, Noordwijk, The Netherlands, June 1995.

3. Parkes and Price 1994, "DSP-Links Study Final Report", Technical Report TR 0104, Matra Marconi Space, Bristol, UK, Oct 1994.

4. Liebstuckel et al 1997, "SMCS User Guide", DIPSAP-II-DAS-31-06, Open Microprocessor Systems Initiative, Dornier Satellitensysteme, 1997.

5. Christen, "APPS : Standardisation of Interfaces", APPS-TN-DSS-0003, Daimler-Benz Aerospace, 1997

6. Postulka et al, 1995 "System Architecture for Solid State Mass Memory, Final Report", ESA contract No. 10971/94/NL/FM(SC), Daimler-Benz Aerospace, SSMM-DOR-WR-5000, Sept 1995.

7. Rastetter and Meier 1996, "Simple Interprocessor Communication Protocol Specification", DIPSAP-II-DAS-31-01, Open Microprocessor Systems Initiative, Dornier Satellitensysteme, 1996.

8. Eonic Systems , "Virtuoso the SoftStealth RTOS for DSP and ASIC Cores", Technical Brief, TB201-0398, Eonic Systems, 1998.

9. IEEE Computer Society, "IEEE Standard for a High Performance Serial Bus", IEEE Standard 1394-1995, IEEE, August 1996.

10. Johnson and Graham, "High-Speed Digital Design – A Handbook of Black Magic", Prentice-Hall, 1993, ISBN 0-13-395724-1.

11. Petty C and Pearson T, "Designing with PECL (ECL at +5.0V)", Motorola Application Note AN1406, Motorola Inc., 1996.

12. Telecommunications Industry Association, "Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits", ANSI/TIA/EIA-644-1995, March 1996.

13. IEEE Computer Society, "IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI)", IEEE Standard 1596.3-1996, IEEE, July 1996.

14. National Semiconductor, "DS90C031 LVDS Quad CMOS Differential Line Driver", Data Sheet, October 1994.

15. National Semiconductor, "DS90C032 LVDS Quad CMOS Differential Line Receiver", Data Sheet, October 1994.

16. Gottschlag D and Aulton J, " ENVISAT-1 EMC Requirements Specification", PO-RS-DOR-PL-0006, Issue 2, Dornier GmbH, February 1994.

17. Konig W, "Rosetta EMC Requirements Specification", RO-DSS-RS-1002, Issue 1A, Daimler-Benz Aerospace, August 1997.

18. Texas Instruments, "SN65LVDS31 Quadruple High-Speed Differential Driver", Data Sheet, July 1997.

19. Texas Instruments, "SN65LVDS32 Quadruple High-Speed Differential Receiver", Data Sheet, July 1997.

20. LSI-Logic http://www.lsil.com/products/5_8d2.html

Table 3 : Does LVDS Meet The Requirements			
Ref.	Title	Requirement Summary	LVDS
R1.1	Maximum signalling Rate	> 100Mbaud	√ Expected (TBC)
R1.2	Minimum Signalling Rate	< 0.1 x Maximum Signalling Rate	√ Depends only on 1355 encoder and decoder
R1.3	Maximum Cable Length	> 10m at 100 Mbaud	√ Expected (TBC)
R2.1	Conducted Emission	TBD	√ LVDS is a balanced system and should exhibit good EMC
R2.2	Conducted Susceptibility	Immunity to ±360mV 1kHz. sq. wave	√ LVDS is a balanced system and should exhibit good EMC (TBC)
R2.3-1	Radiated Emission, Electric Field	< 40dBuV/m rms (10kHz - 1GHz, narrow band)	√ LVDS is a balanced system and should exhibit good EMC (TBC)
R2.3-2	Radiated Emission, Electric Field	< 60dBuV/m rms (1GHz - 10Ghz, narrow band)	√ LVDS is a balanced system and should exhibit good EMC (TBC)
R2.3-3	Radiated Emission, Electric Field	< 70dBuV/m rms (10kHz - 1GHz, broad band)	√ LVDS is a balanced system and should exhibit good EMC (TBC)
R2.4-1	Radiated Susceptibility, Electric Field	immunity to 1 V/m rms (14kHz - 1 GHz, 1kHz sq.wave)	√ LVDS is a balanced system and should exhibit good EMC (TBC)
R2.4-2	Radiated Susceptibility, Electric Field	immunity to 20V/m rms (1GHz - 40GHz, Pulsed 1kHz PRF)	√ LVDS is a balanced system and should exhibit good EMC (TBC)
R2.5-1	Radiated Emission, Magnetic Field	< 50dBpT (30Hz - 50kHz, narrow band)	√ LVDS is a balanced system and should exhibit good EMC (TBC)
R2.5-2	Radiated Emission, Magnetic Field	< 200nT (DC)	√ LVDS is a balanced system and should exhibit good EMC (TBC)
R2.6-1	Radiated Susceptibility, Magnetic Field	< 136dBpT (30Hz-500Hz)	√ LVDS is a balanced system and should exhibit good EMC (TBC)
R2.6-2	Radiated Susceptibility, Magnetic Field	< 120dBpT (500Hz-50kHz)	√ LVDS is a balanced system and should exhibit good EMC (TBC)
R2.6-3	Radiated Susceptibility, Magnetic Field	< 155dBpT (DC, Earth Field)	√ Earth Field
R3.1	ESD Rating	> 3000 V	√ All LVDS devices are specified to this level or higher
R4.1	Bit Error Rate (BER)	$< 10^{-12}$ over 10m	√ Expected (TBC)
R5.1	Total Dose	> 100krad (Si)	(1)
R5.2	Single Event Upset	> 30 MeV/mg/cm^2	(1)
R5.3	Latch-UP	> 100 MeV/mg/cm^2	(1)
R6.1	Link Power Consumption	< 0.1 W (uni-directional Link)	√ Calculated as < 0.05W
R7.1	Receiver Inputs Open	Known output state, no oscillation	√ Internal fail-safe resistors
R7.2	Receiver Inputs shorted	Known output state, no damage to receiver	√ Internal fail-safe resistors
R7.3	Driver Outputs Open	No damage to driver	√ Current limited outputs
R7.4	Driver Outputs Shorted	No damage to driver	√ Current limited outputs
R7.5	Driver Powered, Receiver Not Powered	No damage to driver or receiver	√ Current limit on outputs should prevent thermal damage in receiver
R7.6	Driver Not Powered, Receiver Powered	No damage to driver or receiver and known output state	√ Internal fail-safe resistors in receiver
R7.7	Driver Tri-State	Possible to tri-state driver	√ Available devices have this facility
R8.1	Driver / Receiver Packaging	Small outline package with multiple drivers and/or receivers	√ Available devices are small outline with multiple drivers or multiple receivers in a single package
R8.2	Driver / Receiver Integration	Possible to integrate with encoder etc.	√ LVDS can be implemented in CMOS, GaAs, etc.
R8.3	Line Termination	No more than three components	√ Single resistor
R8.4	Driver/Receiver Supply Voltage	Same Vcc as system	√ Both 5V and 3.3V devices available
R9.1	Non-Ferrous Materials	No ferrous material to be used	√ TBC that devices do not contain ferrous materials
R10.1	Galvanic Isolation	Possible to galvanically isolate two systems connected by link	√ Using TI patented method with bus hold devices

Notes: (1) If necessary (i.e. current devices are not sufficiently radiation tolerant) the LVDS drivers and receivers could be manufactured in a radiation tolerant technology.